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LOW JITTER INPUT BUFFER WITH SMALL INPUT SIGNAL SWING

Background of the Invention

Field of the Invention

[0001] The present invention generally relates to an interface circuit, and particularly to a low jitter input buffer.

Description of Related Art

[0002] Major design efforts have been directed at circuit design techniques involving input circuits for memory devices. A number of solutions have been proposed.

[0003] U.S. Patent 5,978,310 (Bae et al) describes an input buffer for a DRAM memory device, which removes noise from the row address strobe. The device has a data output enable, which can be delayed for a predetermined time, and which also produces a control signal for the output. There is also a buffer output for producing the noise free input according to the control signal.

[0004] U.S. Patent 6,002,618 (Komarek et al) discloses an NMOS input receiver circuit for a read only memory. It includes a feedback loop to control hysteresis. There is a second stage and an additional output for the receiver. Switching noise from inside the memory is isolated and cannot be fed back into the receiver circuit to affect the TTL voltage levels. Wide, long FET sizes are used to minimize manufacture variations in the receiver switching levels.

[0005] What is still needed is a mechanism by which an input buffer works in the presence of ground noise, specifically how capacitance can be used to reduce such noise for a memory input circuit.

Summary of the Invention

[0006] It is therefore an object of the present invention to provide an efficient circuit design technique for an input buffer receiver for a particular memory device that works to filter ground noise. It is a further object of the invention to provide a means for reducing jitter in an input buffer. This is achieved by attaching a large capacitance to the bias node of the input buffer receiver.

[0007] These and other objects are achieved by an input buffer receiver comprising: a buffer input portion for receiving an input signal; a large capacitor between a bias node and a lower supply voltage VSS, and a buffer output portion for producing an output signal. Furthermore, in the

input buffer receiver, the biasing voltage of the bias node is charge coupled to the lower voltage source. This results in a quicker response time for the output signal.

Brief Description of the Drawings

[0008] The foregoing and other objects, aspects, and advantages will be better understood from the following detailed description of a preferred embodiment of the invention, with reference to the drawings, in which:

[0009] FIG. 1 is a diagram of an input buffer receiver according to the prior art.

[0010] FIG. 2 is a diagram of an input buffer receiver according to the present invention.

[0011] FIGS.3A-B show the timing diagrams of the input buffer receiver of the present invention and the definitions of JITTER_RISE and JITTER_FALL.

[0012] FIGS. 4A-B illustrate the workings of capacitor CHC to reduce JITTER_RISE and JITTER_FALL.

Detailed Description of the Invention

[0013] One embodiment of the present invention is provided below with reference to the accompanying diagrams.

[0014] Referring to FIG. 1, the input buffer receiver of the prior art includes a buffer input portion 100 for receiving an input signal SIGNAL_IN and a buffer output portion 200 for producing an output signal SIGNAL_OUT.

[0015] The buffer input portion 100 is comprised of: NMOS transistors N1 and N2, where a lower supply voltage VSS is applied to the source nodes of NMOS transistors N1 and N2, and PMOS transistors P1 and P2, where an upper voltage supply VDD is applied to the source nodes. The gate nodes of transistors P1 and P2 and the the drains of transistors N1 and P1 are connected together to form the biasing node b1. The biasing voltage VB1 is developed at the biasing node b1 as a result of the configuration of transistors P1 and P2. A parasitic capacitor Cp is present from the biasing node b1 to the ground reference node. In the prior art, a reference voltage VREF is applied to the gate of transistor N1, input signal SIGNAL_IN is applied to the gate of transistor N2. Input signal SIGNAL_IN is a low swing signal coming from off chip. The buffer output portion 200 is comprised of a common node for the drain of transistor N2 and drain of transistor P2, which serves as input to inverter I1. The output of inverter I1 is the output signal output SIGNAL_OUT.

[0016] The ground noise (VSS noise), as described above, is developed between the lower supply voltage VSS and the ground reference voltage. The magnitude of the VSS noise affects the delay timing from the input signal SIGNAL_IN to the output signal SIGNAL_OUT. The variation in the delay causes jitter in the rise and fall delays of the buffer and thus slower response times.

[0017] Referring to FIG. 2, the proposed invention is comprised of a similar buffer input portion 101 and a similar buffer output portion 201. The buffer input portion 101 is comprised of: NMOS transistors N11 and N12, where the lower supply voltage VSS is applied to the source nodes of N11 and N12, and PMOS transistors P11 and P12, where an upper supply voltage VDD is applied to the source nodes. The gate nodes of transistors P11 and P12 and the the drains of transistors N11 and P11 are connected together to form the biasing node b11. The biasing voltage VB11 is developed at the biasing node b11 as a result of the configuration of transistors P11 and P12. A parasitic capacitor Cp is present from the biasing node b11 to the ground reference node. A reference supply voltage VREF is applied to the gate of transistor N11, input signal SIGNAL_IN is applied to the gate of N12. In the present invention, a large capacitor CHC is attached between the bias node b11 and the lower supply voltage VSS. The buffer output portion 201 is comprised of a common node for the drain of transistor N12 and the drain of transistor

P12, which serves as input to inverter I11. The output of inverter I11 is the output signal SIGNAL_OUT1 of the invention.

[0018] The large capacitance CHC is in series with the parasitic capacitor Cp of the input buffer receiver transistors N11, P11, and P12. The large capacitor CHC, as connected, is designed to have an extremely large capacitance relative to the parasitic capacitor Cp such that the bias voltage VB11 essentially follows the voltage changes in the lower supply voltage VSS preventing the effects of the VSS noise. This coupling ratio is determined by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor CHC.

Cp is the capacitance value of the parasitic capacitor Cp.

[0019] Because of its large coupling ratio (very close to 1), the capacitor CHC essentially charge couples the biasing voltage VB11 bias node b11, to the lower supply voltage VSS, of devices N11 and N12. This forces the transistors N11 and N12 to activate and deactivate essentially

simultaneously, allowing for a quicker response time on output signal SIGNAL_OUT1.

[0020] FIGS. 3A-B are diagrams of timed operation showing the input signal SIGNAL_IN, the lower supply voltage VSS, and the output signal SIGNAL_OUT1 of the proposed invention. It should be noted that the input signal SIGNAL_IN is defined as VIH=VREF+350mv and VIL=VREF-350mv, and VSS is 200mv. The output signal SIGNAL_OUT1 is defined by the delay times DELTA1 or DELTA2, when input signal SIGNAL_IN rises, and the delay times DELTA3 or DELTA4, when the input signal SIGNAL_IN falls. The delay time DELTA1 is defined as the delay from the rising edge of input signal SIGNAL_IN to the rising edge of output signal SIGNAL_OUT, when VSS=200mv. It is the delay on output signal SIGNAL_OUT1 when transistor N12 sees VSS noise and turns on weakly. The delay time DELTA2 is defined as the delay from the rising edge of input signal SIGNAL_IN to the rising edge of output signal SIGNAL_OUT1, when VSS=0v. It is the delay of the output signal SIGNAL_OUT1 when transistor N12 does not see VSS noise and turns on strongly. The delay time DELTA3 is defined as the delay from the falling edge of input signal SIGNAL_IN to the falling edge of output SIGNAL_OUT1, when VSS=0v. It is the delay of the input signal SIGNAL_OUT1 when transistor N12 does not see VSS noise and turns off weakly. DELTA4 is defined as the delay from the falling edge of input

signal SIGNAL_IN to the falling edge of output signal SIGNAL_OUT1, when VSS=200mv. It is the delay seen on output signal SIGNAL_OUT1 when transistor N12 sees VSS noise and turns off strongly. By definition, the delay times DELTA2 and DELTA4 are smaller than the delay times DELTA1 and DELTA3. The rise time jitter JITTER_RISE is the difference between the delay times DELTA1 and DELTA2 when the input signal SIGNAL_IN rises and the fall time jitter JITTER_FALL is the difference between the delay times DELTA3 and DELTA4 when input signal SIGNAL_IN falls. The intent of the invention large capacitor CHC is to reduce rise time jitter JITTER_RISE and fall time jitter JITTER_FALL by primarily having transistors P12 and N12, activate, in the presence or absence of ground noise, almost simultaneously.

[0021] FIGS. 4A-B illustrate the workings of large capacitor CHC. In Fig. 4a, the large capacitor is shown in series with the parasitic capacitor Cp. The large capacitance coupling ratio of the large capacitor CHC versus the capacitance of the parasitic capacitor Cp creates a charge coupling of the bias node, b11, of the input buffer receiver, to the lower supply voltage VSS, of the input buffer receiver. This results in a quicker response time for a input signal SIGNAL_OUT1.

[0022] While the invention has been described in terms of the preferred embodiments, those skilled in the art will recognize that various changes in form and details may be made without departing from the spirit and

scope of the invention. The present invention covers modifications that fall within the range of the appended claims and their equivalents.

[0023] While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

[0024] What is claimed is: